Sep 25, 2002

GAFE

GLAST ACD Front End Electronics ASIC

Test Report

Design Version Proto 1-1 (GAFE1)

Sep 25, 2002
(earlier rev dated: sep 17, 02)

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Scope:

The scope of this document is to describe the test results of the GLAST ACD prototype ASIC (also referred to as GAFE1) for the Front End Electronics. This chip was fabricated in Ag/HP 0.5 um CMOS process, wire bonded into a ceramic chip carrier and tested using a Test Board built on a vector board. Therefore there is a scope for improvement, however the test results are good enough to demonstrate the performance of the chip.

Revisions / Update in this edition:

Compared to the earlier version dated Sep 17, 02, this test report includes the testing of GAFE1 with PMT (Section 4.13). The intent of these tests were to check the performance of the ASIC in a more real type environment using a PMT and to go up to full 1000 MIPs and especially check the charge splitting performance.

Table of Contents

1. Introduction:

This Document describes the test the configuration, methods and results of functional testing of the GLAST ACD Front-end Electronics ASIC (GAFE) version Proto 1_1, (GAFE1).

2. GAFE description

The GAFE ASIC is the front-end analog interface to the PMTs providing signal conditioning of the ionizing event signals for subsequent digitization and processing. The GAFE ASIC provides amplification, shaping, discrimination and timing functions for signal processing by the ACD. The GAFE ASIC is described in more detail in another document that describes the ASIC requirements and architecture.

Four of the GAFE Proto 1_1 ASIC dies were mounted and bonded in 42 pin ceramic, surface mount, 48 pin packages. One of the dies was not successfully bonded leaving three ASICs available for testing.

3. Test Configuration

The test setup configuration consisted of two breadboard implementations of the test circuit on perforated vector boards. Test board 1 was constructed on standard perfboard with one GAFE1 ASIC directly soldered into the circuit to minimize lead length. The second test board was constructed on perfboard using a "clamshell" chip carrier allowing the easy change of ASICs.

For testing, standard lab equipment was used, like the HP 6214a power supply, BNC BH-1 Tail Pulse Generator, BNC PB-4 Tail Pulse Generator, HP 54815a Digital Oscilloscope, HP 8013b Pulse Generator, Fluke 8842a multimeter.

4.0 Functional Tests

The various tests performed are described next.

4.1 Power

The test boards were powered by 3.3v dc. Vcc (analog supply) and Vdd (digital supply) are derived from the 3.3v supply and isolated from each other through RC filtering of 100 ohms and 10uF tantalum paralleled with 0.1 ceramic capacitors. The current draw by both the analog and digital portions of the ASIC produced a voltage drop across the 100 ohm resistor. The current draw of Both ASICs tested was consistent.

	V supply	I supply (mA)	Vcc (at ASIC)	Icc - ma	Vdd (at ASIC)	Idd - ma
Board 1	3.3	10.44	3.24	0.6	2.28	10.2
Board 2	3.25	10.6	3.25	0.5	2.29	10.1

Analog Power: 3.24 v * 0.6ma = 1.994 mw
Digital Power : 2.28 v * 10.2 ma = 23.256mw

The digital power measured was far in excess of its expected value, the reason for this was traced to error in ASIC layout and faulty cell used from the Tanner Library.

4.2 Shaping Amp

Test charge was injected through a 33Pf capacitor by supplying a square wave of 50% duty cycle with a time period of 2 ms. The input resistance to the low energy channel (or the High gain channel) was 12 K, and that to the high energy channel (or the low gain channel) was 570K ohm. A lower resistance of 570 K instead of 1.2 Meg was used as the pulser could output only 10 v pulses and with 1.2 Meg, 20 V pulses are required to go full scale.

Shaping amp gain and timing data was measured using the HP oscilloscope with 10x probes, ac couple with 1meg impendence.

The Peaking time was measured to be around 6.2 us compared to the designed value of 3us. This was attributed to the fabricated Nwell resistances being twice the value.

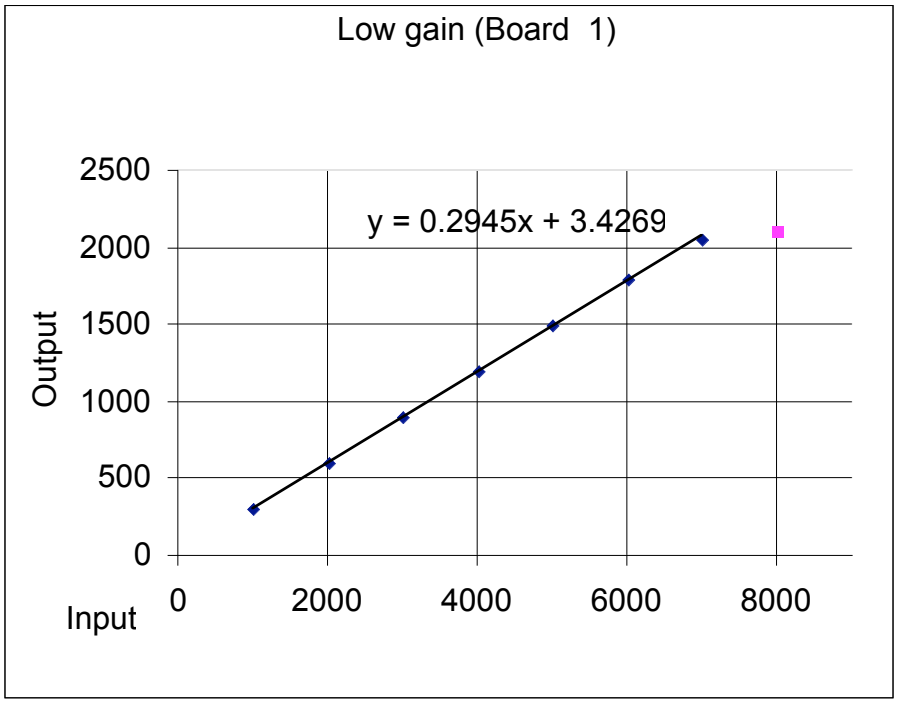
Shaping Amp Gain, Low Gain Channel (Board 1):
Temp: + 25 C

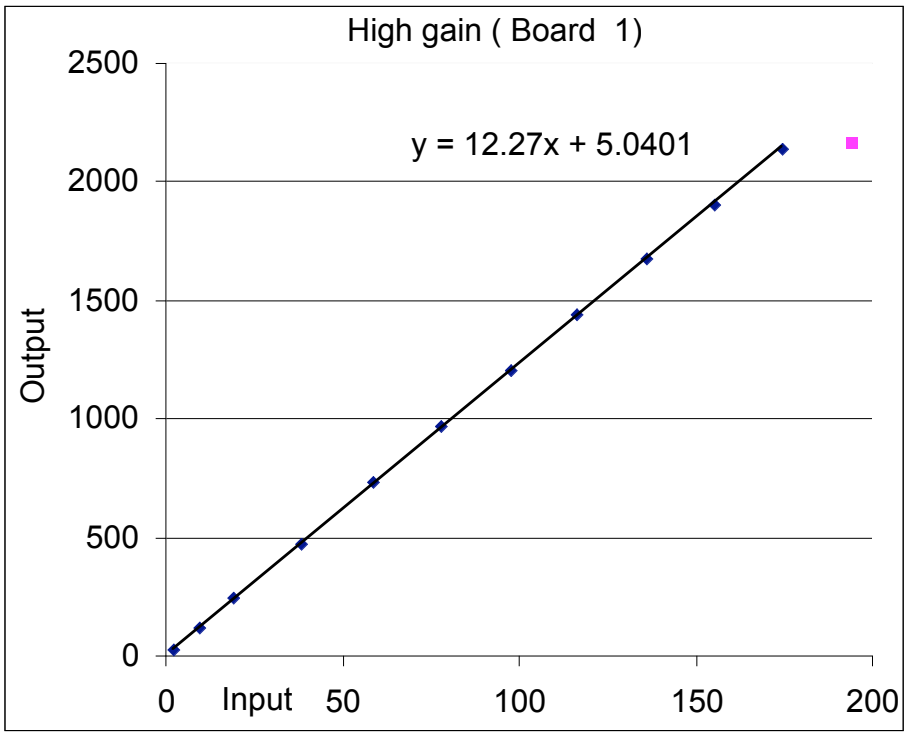
MIP	Input Charge (PC)	Input V (mv)	SA Low Gain (MV)
51.820313	33.165	1005	292
104.25938	66.726	2022	591
155.20313	99.33	3010	896
206.92031	132.429	4013	1195
258.37969	165.363	5011	1490
310.50938	198.726	6022	1788
361.35	231.264	7008	2046
413.47969	264.627	8019	2094
464.78438	297.462	9014	2094

Shaping Amp Gain, High Gain Channel (Board 1):
Temp: + 25 C

MIP	Input Charge (PC)	Input V (mv)	SA High Gain mv
0.1026094	0.06567	1.99	23.45
0.4846875	0.3102	9.4	116.3
1.0003125	0.6402	19.4	241
1.9748438	1.2639	38.3	474
3.0164063	1.9305	58.5	729
4.0167188	2.5707	77.9	966
5.0273438	3.2175	97.5	1207
5.9967188	3.8379	116.3	1440
7.0073438	4.4847	135.9	1676

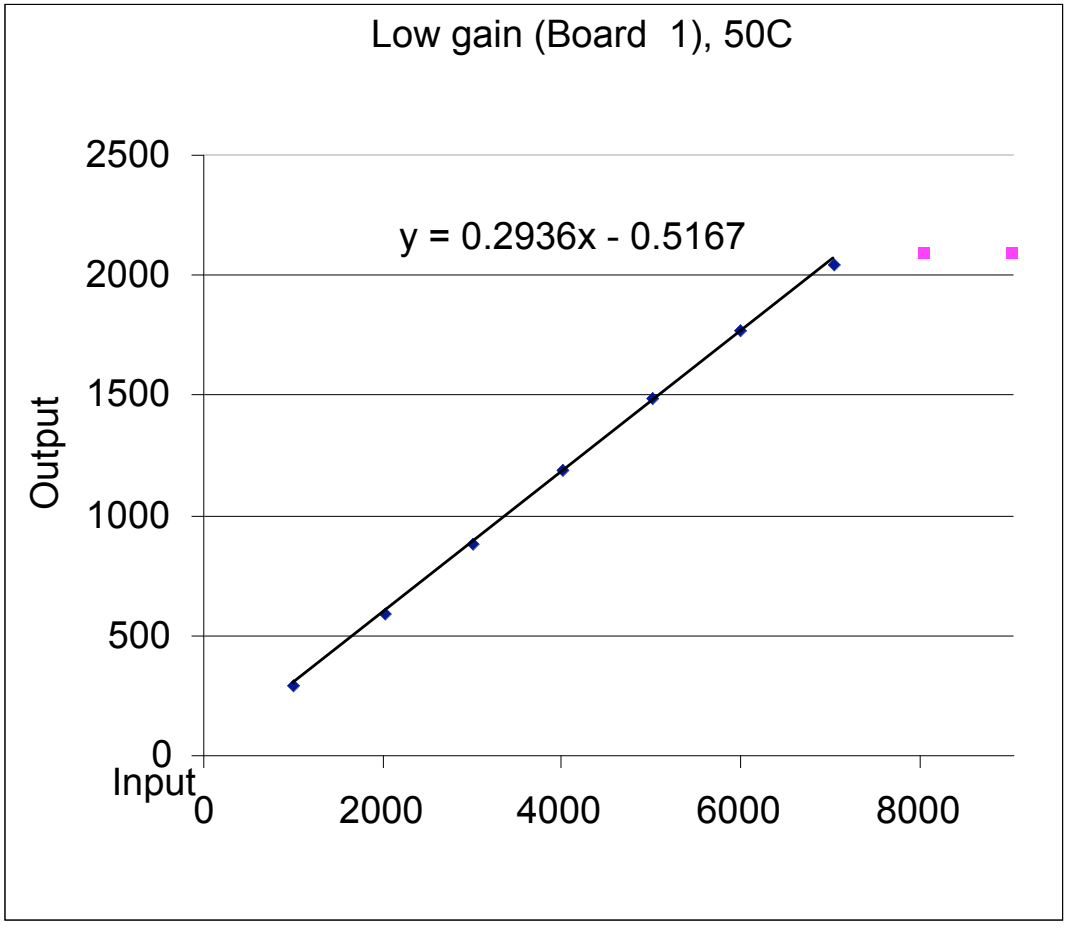
8.0025	5.1216	155.2	1906
9.0079688	5.7651	174.7	2137
10.018594	6.4119	194.3	2161





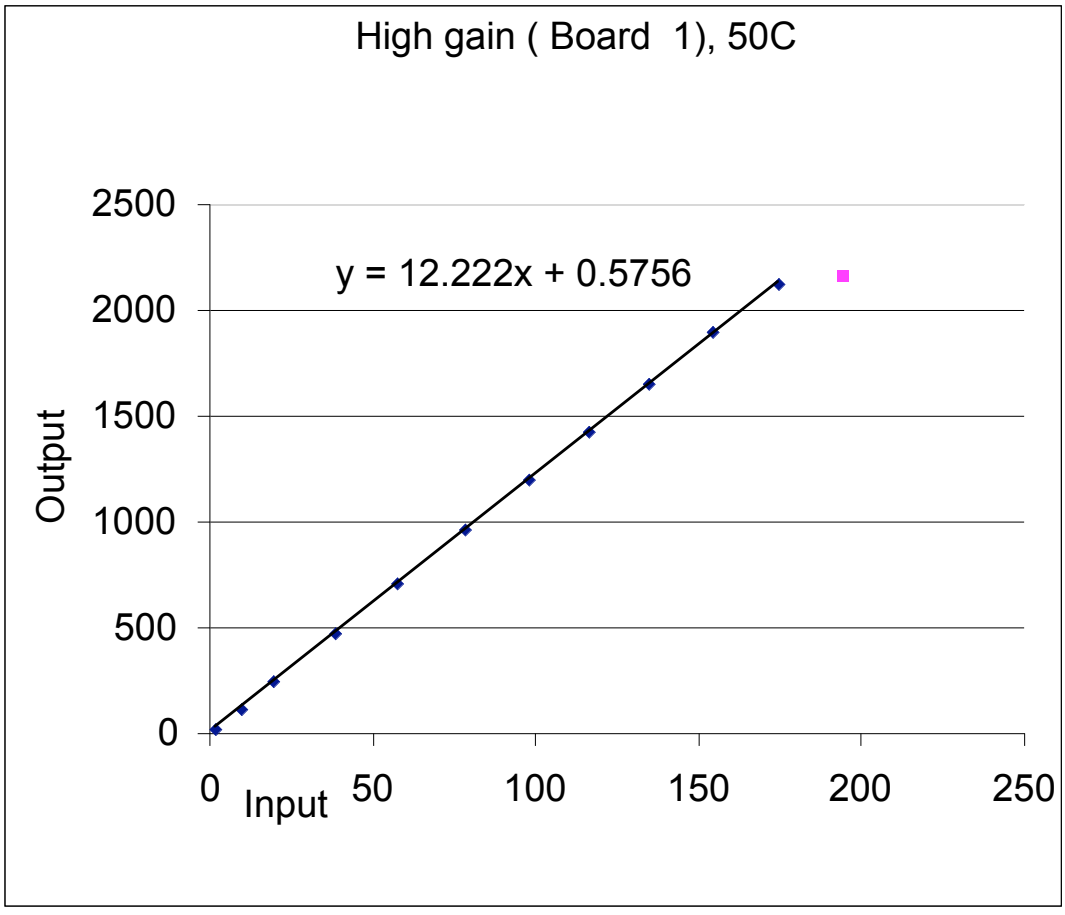
Shaping Amp Gain, Low Gain Channel (Board 1):
Temp: + 50 C

MIP	Input Charge - PC	Input (mv)	SA Low Gain (mv)	
52.129688	33.363		1011	293
104.56875	66.924		2028	588
155.61563	99.594		3018	883
207.28125	132.66		4020	1188
258.17344	165.231		5007	1485
309.375	198		6000	1768
362.84531	232.221		7037	2047
414.71719	265.419		8043	2094
465.3	297.792		9024	2094



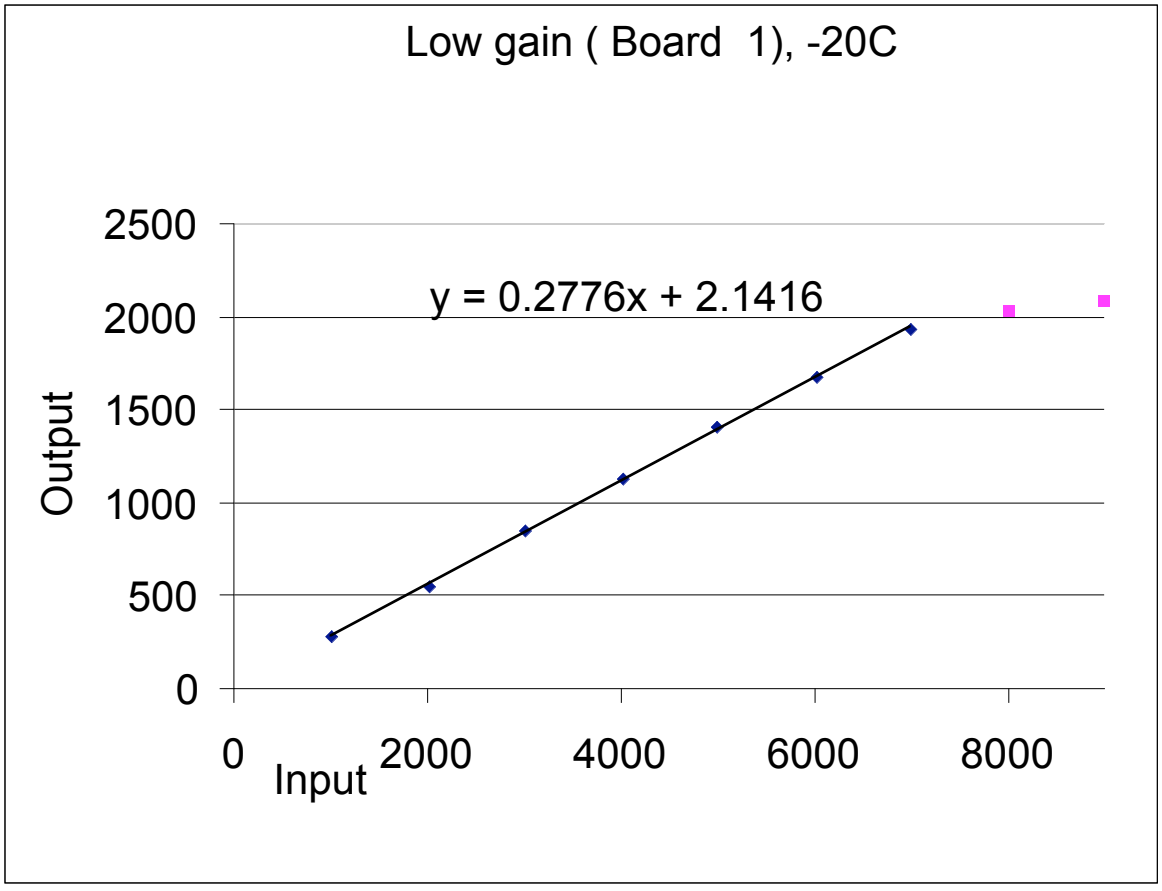
Shaping Amp Gain, High Gain Channel (Board 1):
Temp: + 50 C

MIP	Input Charge PC	Input (mv)	SA High Gain - mv
0.099	0.06336	1.92	21.6
0.4898438	0.3135	9.5	115
1.010625	0.6468	19.6	240.6
1.9851563	1.2705	38.5	471
2.9803125	1.9074	57.8	710
4.0476563	2.5905	78.5	959
5.0428125	3.2274	97.8	1198
6.001875	3.8412	116.4	1423
6.950625	4.4484	134.8	1650
7.9664063	5.0985	154.5	1896
9.0028125	5.7618	174.6	2125
10.018594	6.4119	194.3	2160



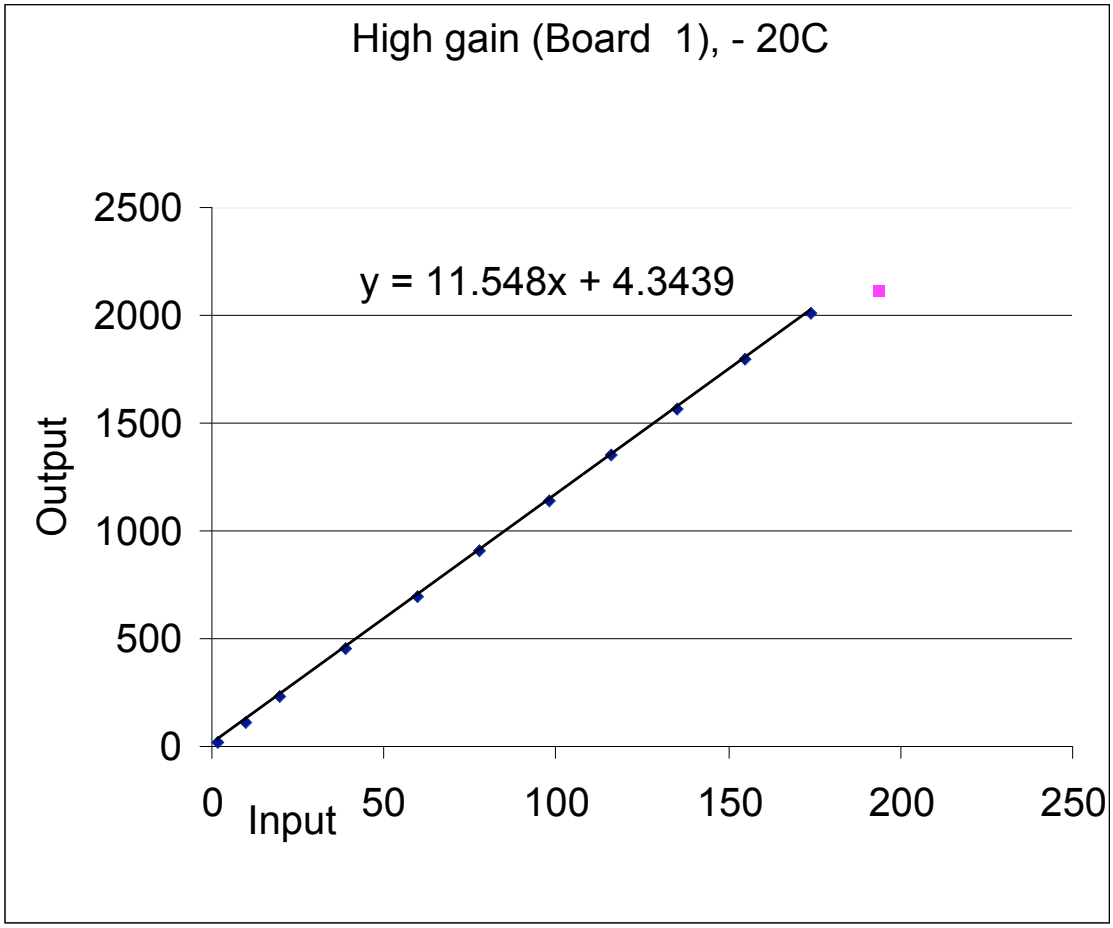
Shaping Amp Gain, Low Gain Channel (Board 1):
Temp: - 20 C

MIP	Input Charge - pc	Input (mv)	SA Low gain V
52.284375	33.462	1014	276
103.79531	66.429	2013	552
154.89375	99.132	3004	847
207.64219	132.891	4027	1129
257.96719	165.099	5003	1401
310.30313	198.594	6018	1670
361.04063	231.066	7002	1934
412.44844	263.967	7999	2030
464.475	297.264	9008	2081



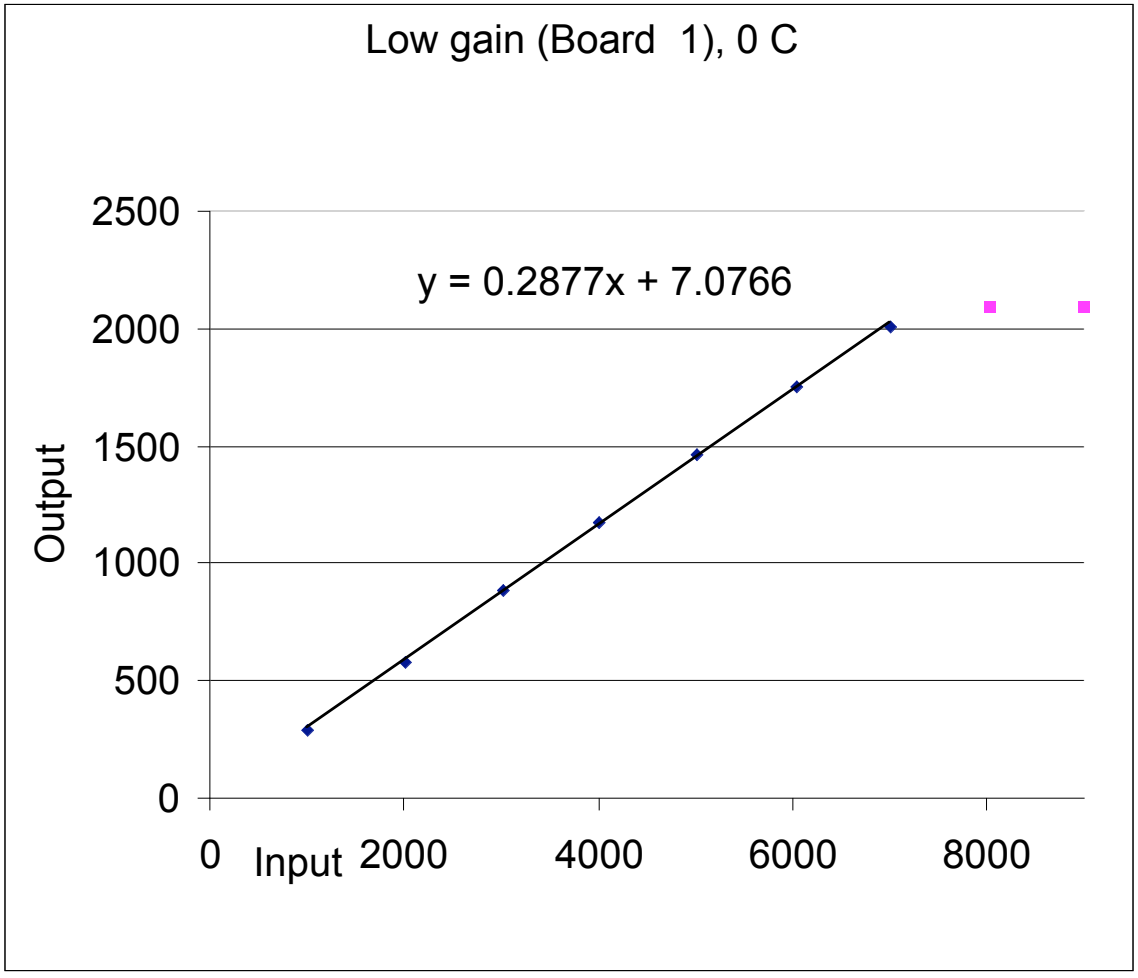
Shaping Amp Gain, High Gain Channel (Board 1):
Temp: - 20 C

MIP	Input Charge PC	Input (mv)	SA High Out, mv
0.0974531	0.06237	1.89	18.6
0.4970625	0.31812	9.64	111.2
1.01475	0.64944	19.68	231.4
2.0057813	1.2837	38.9	455.3
3.0679688	1.9635	59.5	695.8
4.0043438	2.56278	77.66	907.6
5.0479688	3.2307	97.9	1140
5.9915625	3.8346	116.2	1353
6.9815625	4.4682	135.4	1567
7.9921875	5.115	155	1793
8.9770313	5.7453	174.1	2005
9.9825	6.3888	193.6	2110



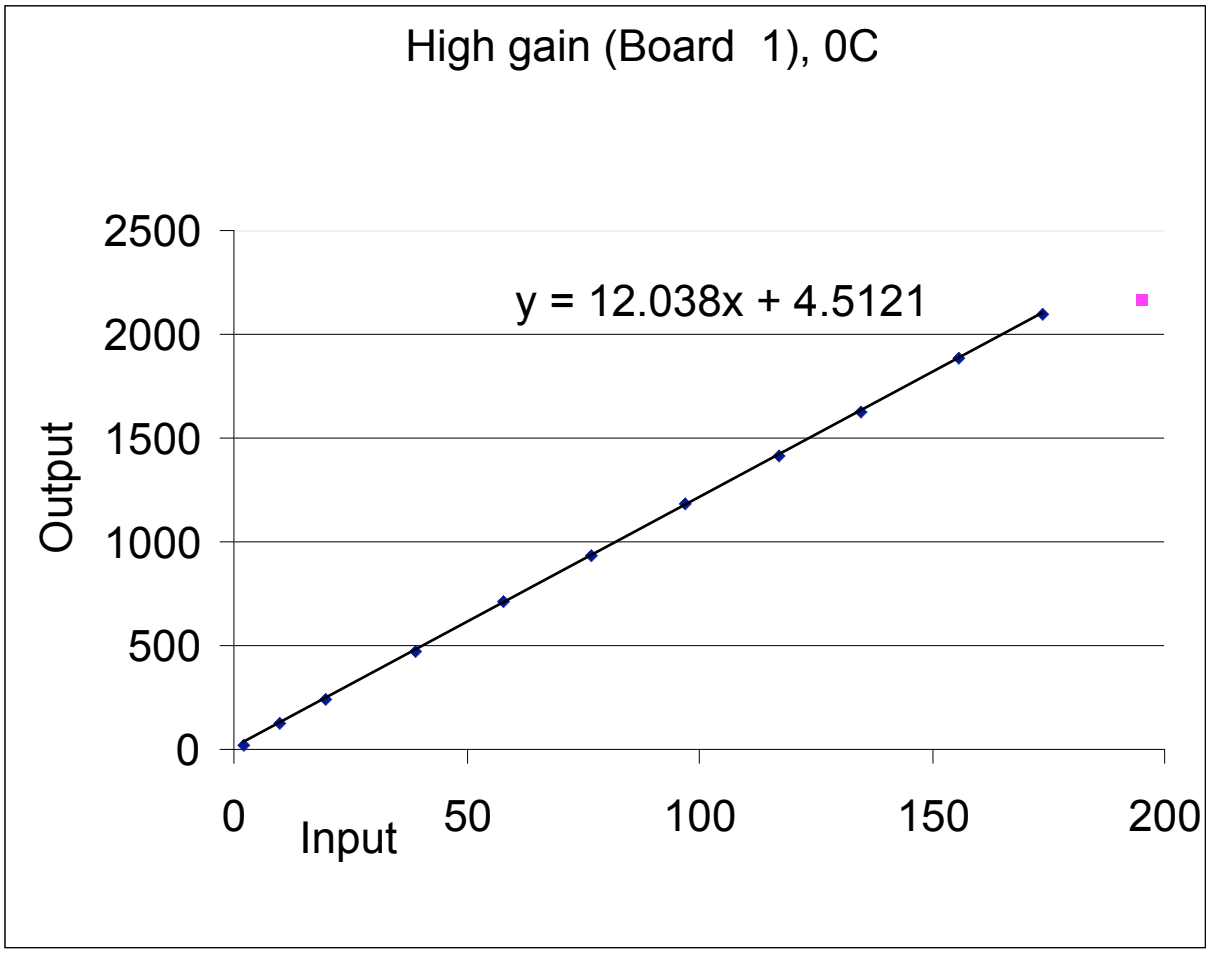
Shaping Amp Gain, Low Gain Channel (Board 1):
Temp: 0 C

MIP	Input Charge PC	Input (mv)	SA Low Gain - mv	
52.026563	33.297		1009	288
104.00156	66.561		2017	578
155.40938	99.462		3014	884
206.97188	132.462		4014	1173
258.37969	165.363		5011	1462
311.54063	199.386		6042	1750
361.45313	231.33		7010	2004
414.5625	265.32		8040	2091
464.52656	297.297		9009	2093

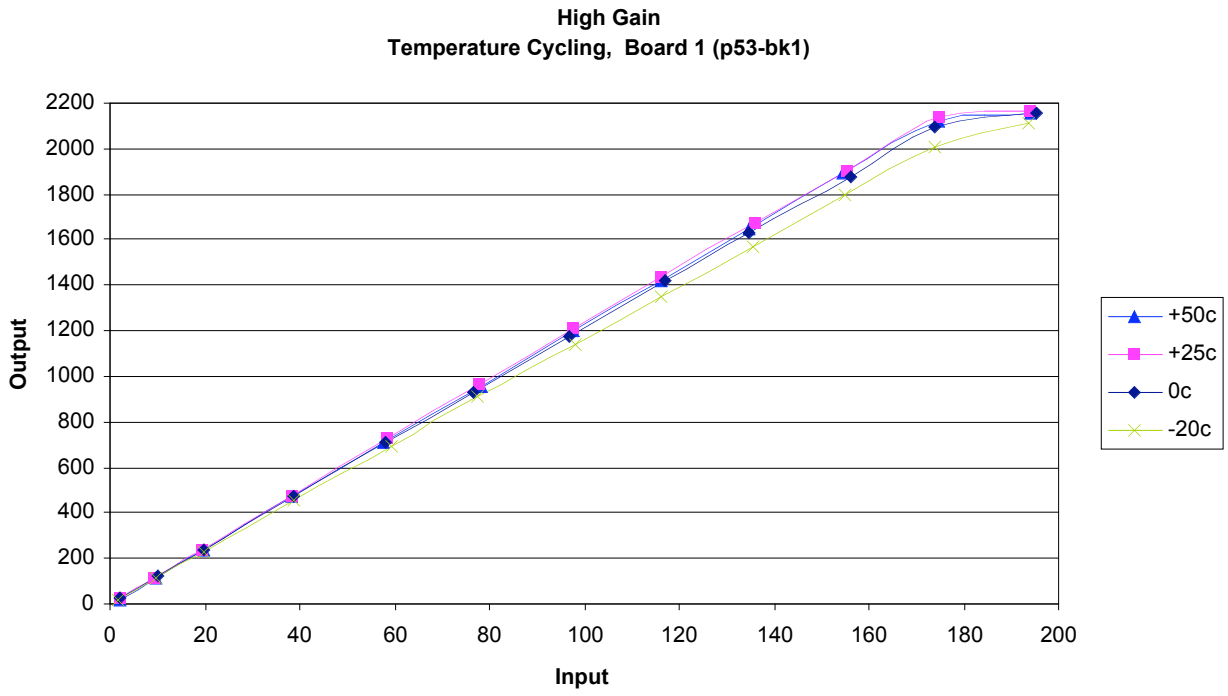


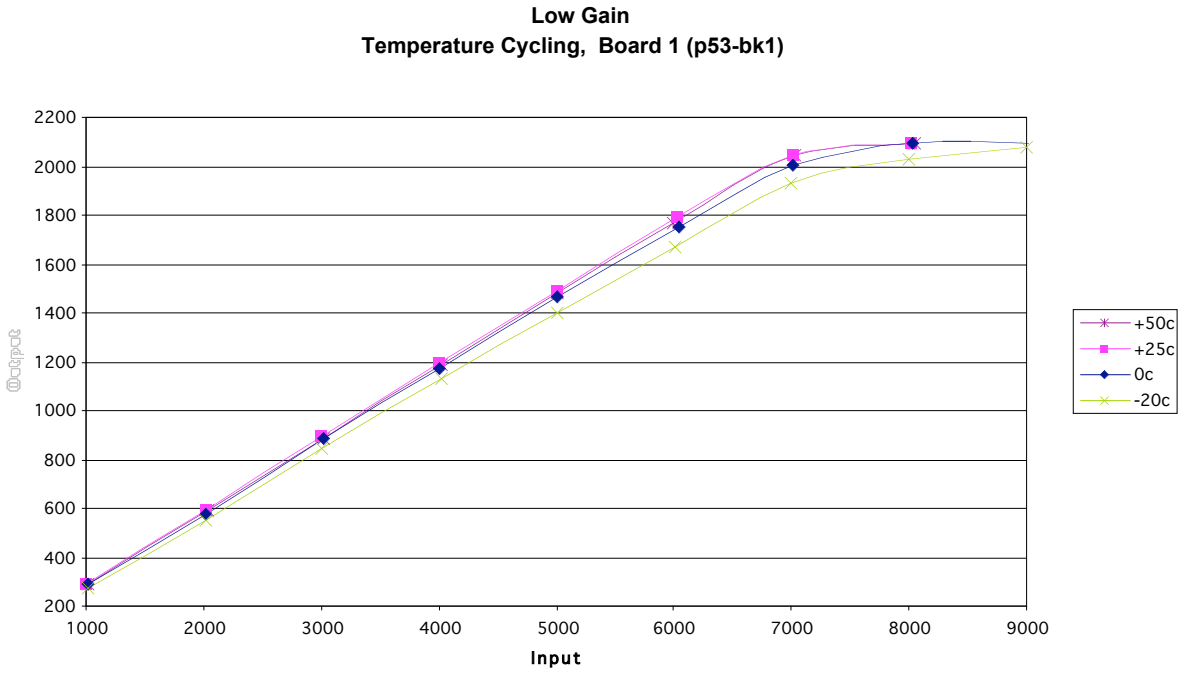
Shaping Amp Gain, High Gain Channel (Board 1):
Temp: 0 C

MIP	Input Charge, PC	Input (mv)	SA High Gain, mv
0.103125	0.066	2	23.21
0.5145938	0.32934	9.98	120.4
1.0209375	0.6534	19.8	241
2.0057813	1.2837	38.9	472
2.9854688	1.9107	57.9	710
3.9548438	2.5311	76.7	932
4.9964063	3.1977	96.9	1178
6.043125	3.8676	117.2	1418
6.950625	4.4484	134.8	1627
8.04375	5.148	156	1880
8.971875	5.742	174	2092
10.065	6.4416	195.2	2159



Below are the graphs showing the temperature variation of gains for the low and high gain channels.





4.3 Charge Splitting:

The charge splitting between two PHA channels can be inferred from the relative gains shown in the preceding plots at various temperatures. These gain ratios are:

Temp 25 C:
12.27 / 0.294 = 41.7

Temp 50 C:
12.22 / 0.2936 = 41.6

Temp -20C:
11.54 / 0.2776 = 41.57

Temp 0C :
12.04 / 0.2877 = 41.8

The resistances used were 12K for the input of low energy (high gain) channel, and 570K for the high energy (low gain) channel. The theoretical ratio of charge splitting is therefore: 570 / 12 = 47.5

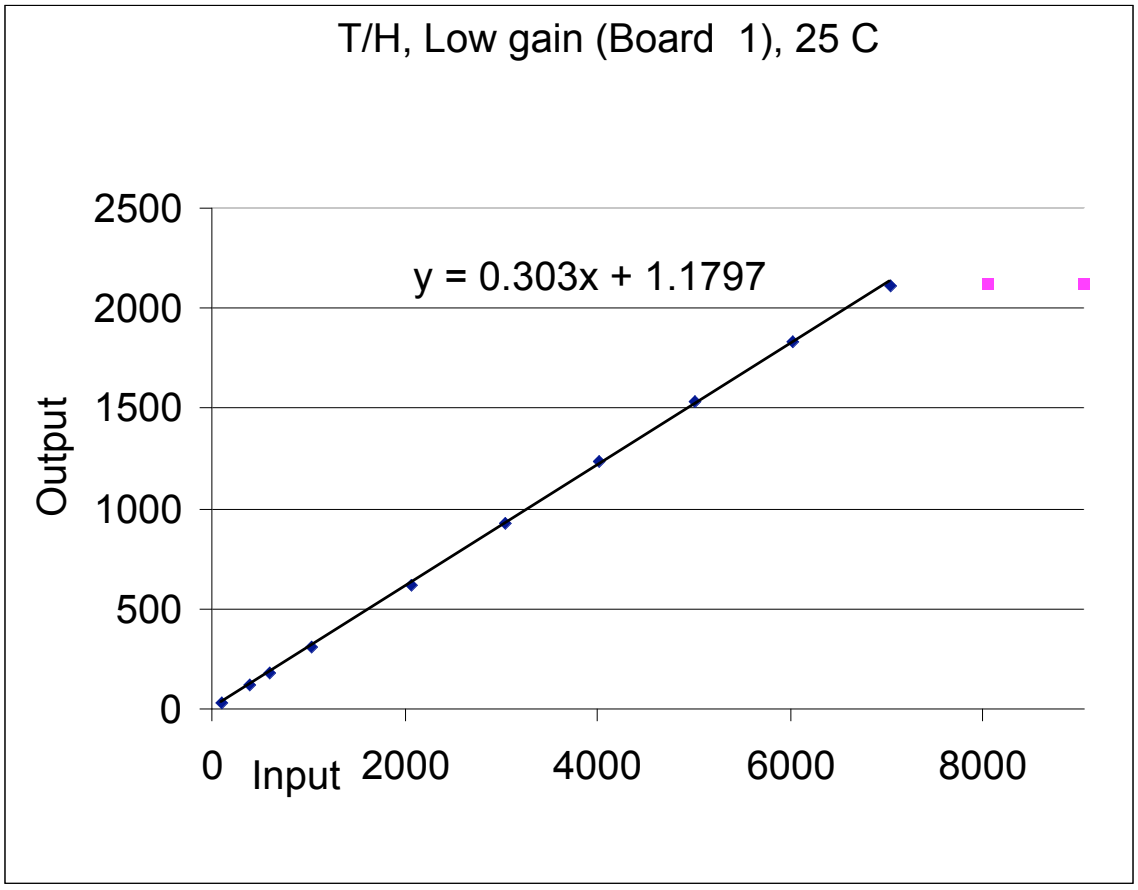
The measured ratio of 41.5 is a little less than the theoretical value of 47.5

4.4 Track and Hold Testing:

Temperature cycling of the Track and Hold output was also done, the gain variations with temperature are depicted in the following plots. For the purposes of testing, the hold pulse was issued at approximately the peak time of the shaping amp output, and the amplitude of the output was measured after a delay of 1.5us to allow for the waveform to settle. The times for the issue of the hold pulse, and the measurement time were then fixed for the entire temperature cycling. That is, if the peaking time changed with temperature, the time for the hold pulse and the measurement time were not changed.

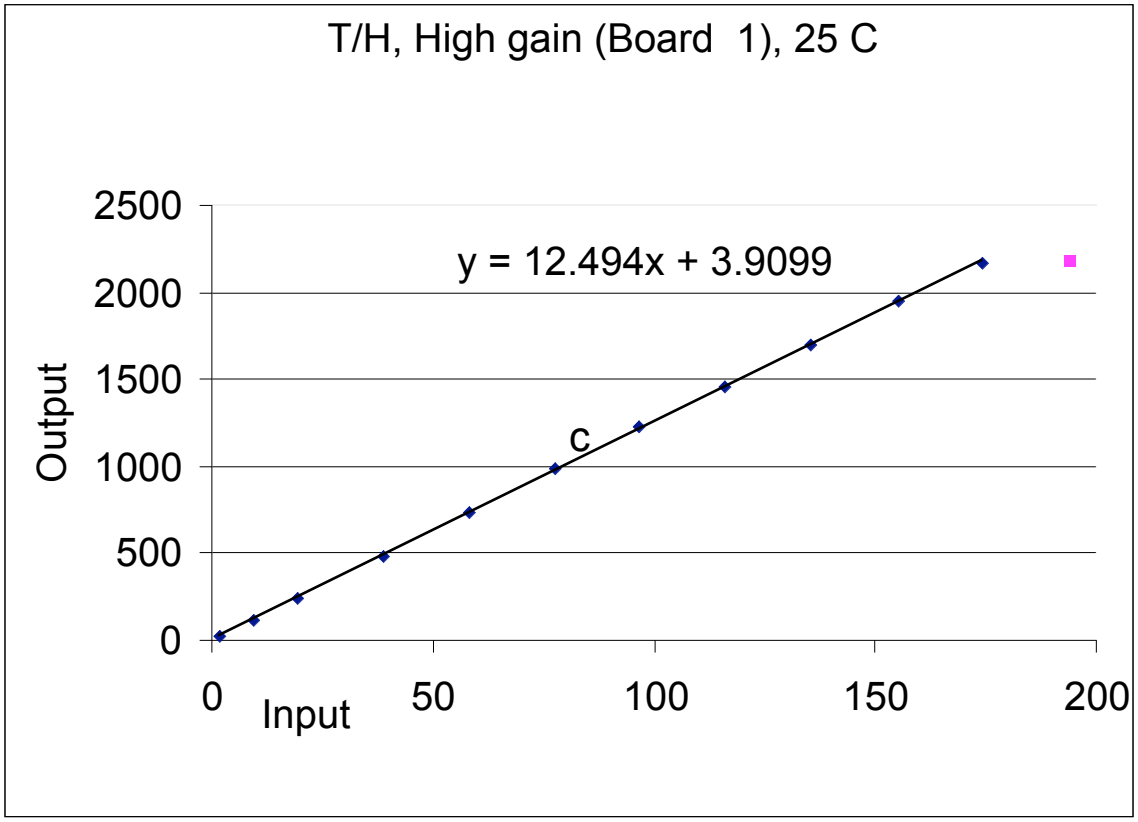
Track and Hold, Low Gain Channel (Board 1):
Temp: 25 C

MIP	Input Charge PC	Input (mv)	T/H Low Gain, mv
5.135625	3.2868	99.6	29.3
20.640469	13.2099	400.3	120.2
30.97875	19.8264	600.8	181.2
53.728125	34.386	1042	309.6
106.57969	68.211	2067	622.5
156.54375	100.188	3036	928
207.59063	132.858	4026	1237
258.68906	165.561	5017	1535
310.81875	198.924	6028	1835
363	232.32	7040	2109
415.18125	265.716	8052	2118
466.125	298.32	9040	2119



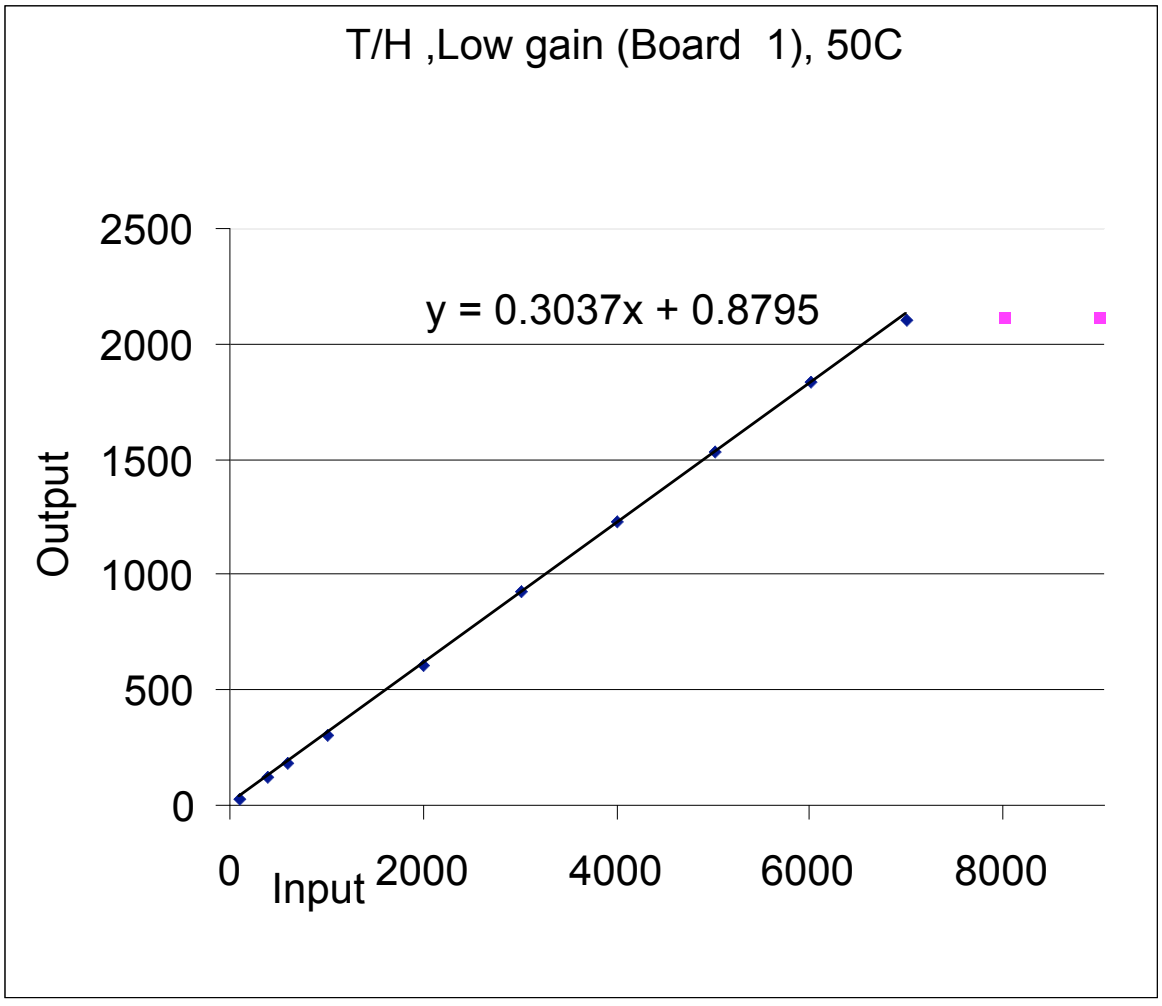
Track and Hold, High Gain Channel (Board 1):
Temp: 25 C

MIP	Input Charge PC	Input (mv)	T/H High Gain, mv
0.1015781	0.06501	1.97	22.8
0.4919063	0.31482	9.54	120.18
0.9972188	0.63822	19.34	245.17
1.9954688	1.2771	38.7	481.93
3.0024844	1.92159	58.23	731.4
4.0084688	2.56542	77.74	983.3
4.9881563	3.19242	96.74	1223
5.9797031	3.82701	115.97	1462
6.9872344	4.47183	135.51	1697
8.0009531	5.12061	155.17	1949
8.9971406	5.75817	174.49	2164
10.001578	6.40101	193.97	2176



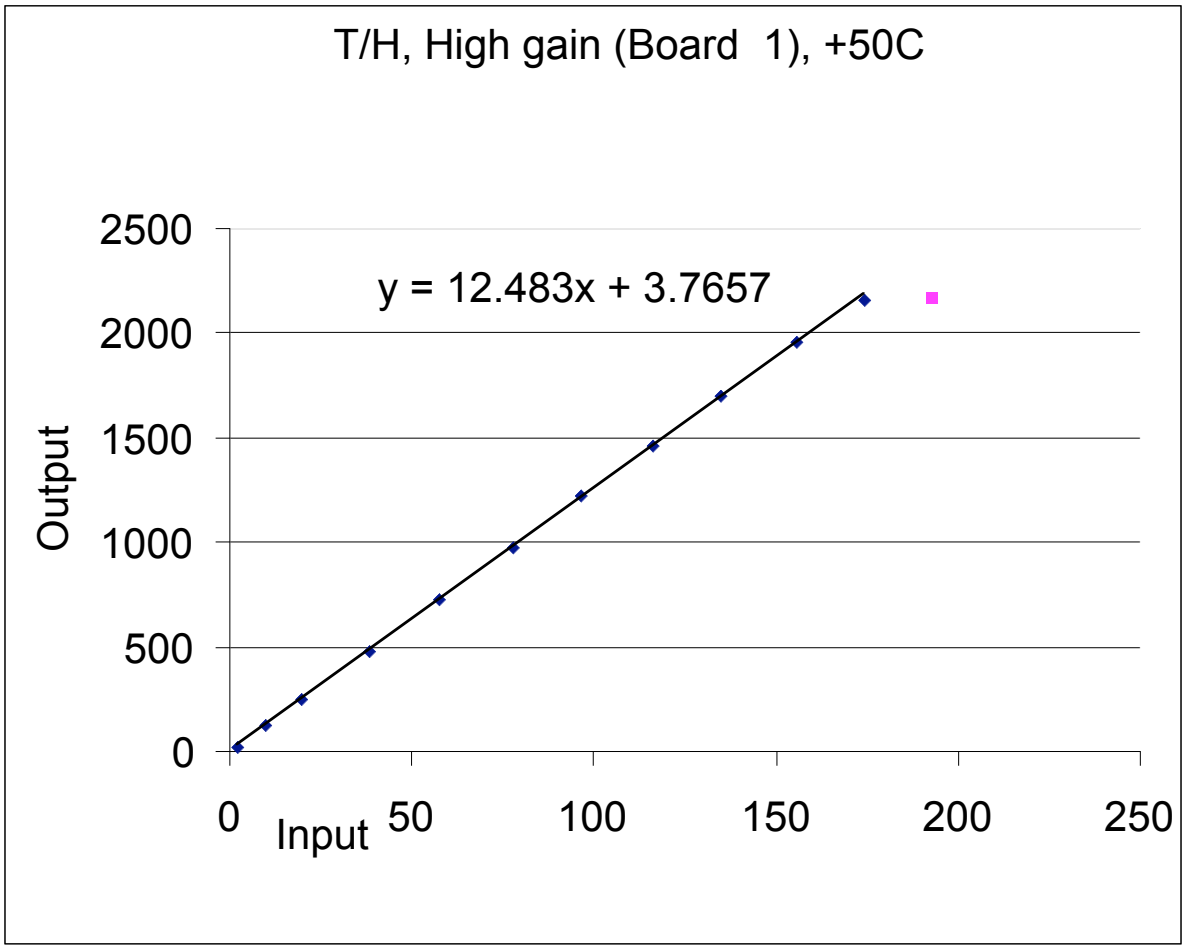
Track and Hold, Low Gain Channel (Board 1):
Temp: 50 C

MIP	Input Charge PC	Input (mv)	T/H Low gain, mv
5.1975	3.3264	100.8	29.8
20.676563	13.233	401	120.2
31.205625	19.9716	605.2	181.9
52.026563	33.297	1009	302.7
103.33125	66.132	2004	605
155.1	99.264	3008	923
206.50781	132.165	4005	1229
258.53438	165.462	5014	1531
309.7875	198.264	6008	1836
361.09219	231.099	7003	2105
413.17031	264.429	8013	2111
464.37188	297.198	9006	2111



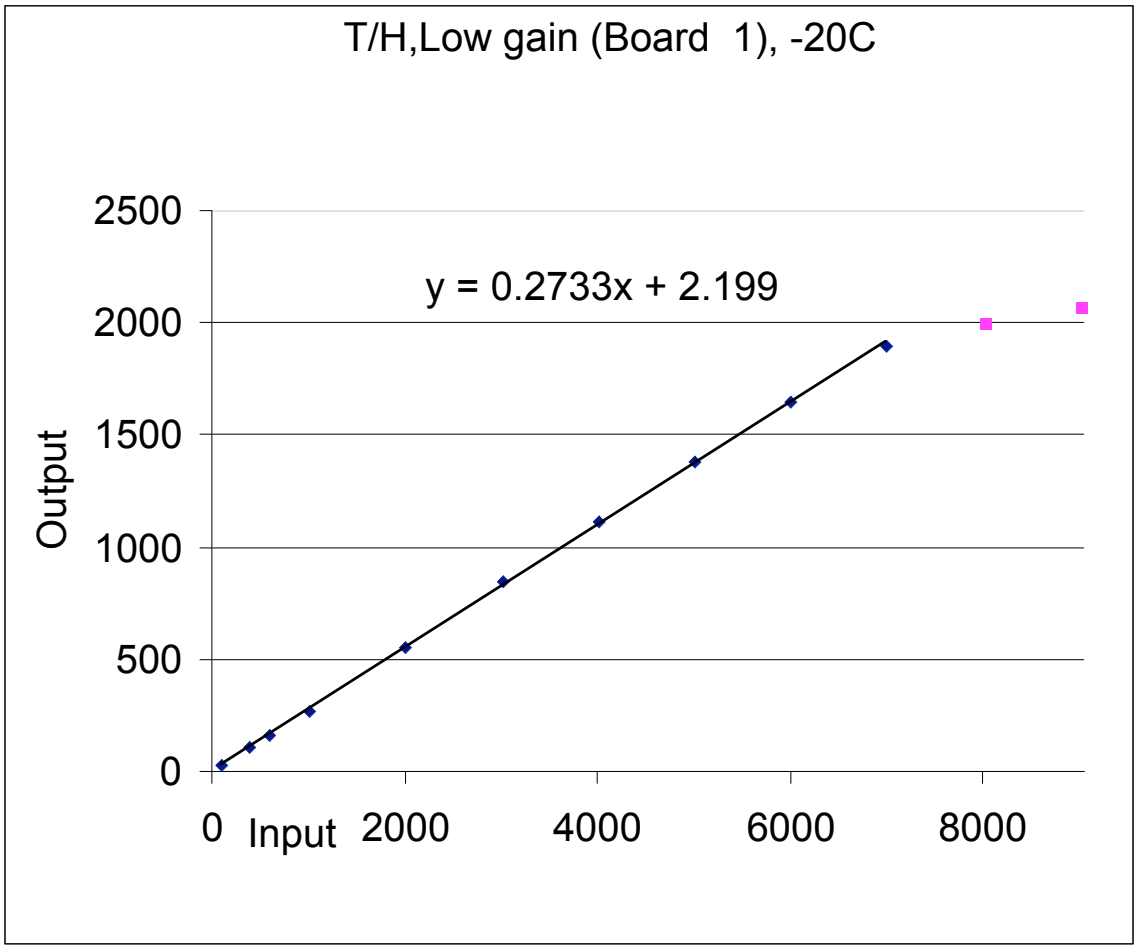
Track and Hold, High Gain Channel (Board 1):
Temp: 50 C

MIP	Input Charge PC	Input(mv)	T/H High Gain, mv
0.1020938	0.06534	1.98	22.5
0.5115	0.32736	9.92	122.6
1.010625	0.6468	19.6	246.2
1.9696875	1.2606	38.2	479.6
2.97	1.9008	57.6	724.6
4.00125	2.5608	77.6	978
4.9860938	3.1911	96.7	1223
6.001875	3.8412	116.4	1460
6.9609375	4.455	135	1696
8.0334375	5.1414	155.8	1957
9.0028125	5.7618	174.6	2159
9.9515625	6.369	193	2169



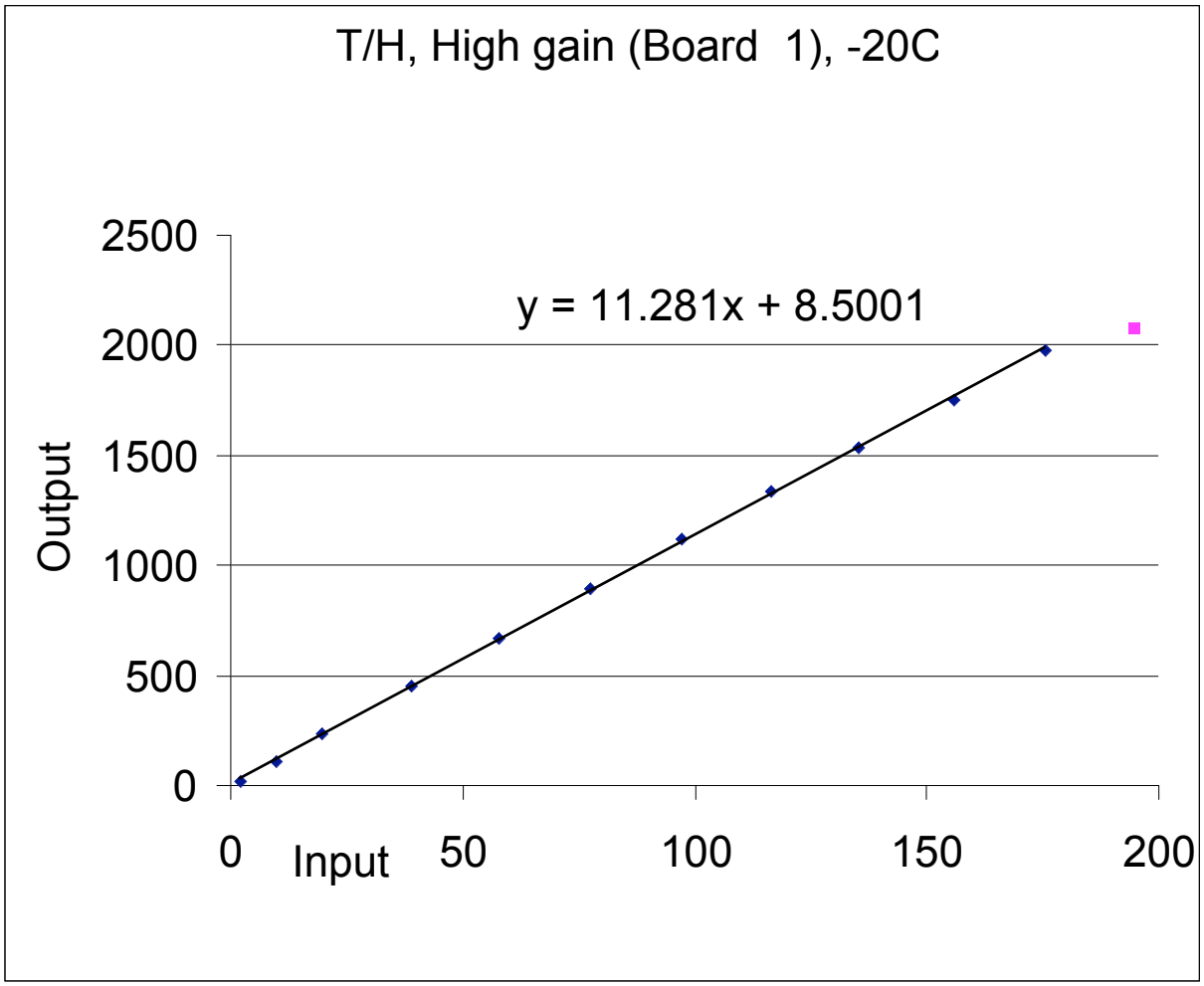
Track and Hold, Low Gain Channel (Board 1):
Temp: - 20 C

MIP	Nom Input (mv)	Input (mv)	T/H, Low gain, mv
5.176875	3.3132	100.4	25.7
20.676563	13.233	401	107.5
30.782813	19.701	597	160.8
52.3875	33.528	1016	271
103.17656	66.033	2001	550.7
155.56406	99.561	3017	844
206.81719	132.363	4011	1115
258.12188	165.198	5006	1375
309.94219	198.363	6011	1644
361.04063	231.066	7002	1897
414.71719	265.419	8043	1994
465.7125	298.056	9032	2060



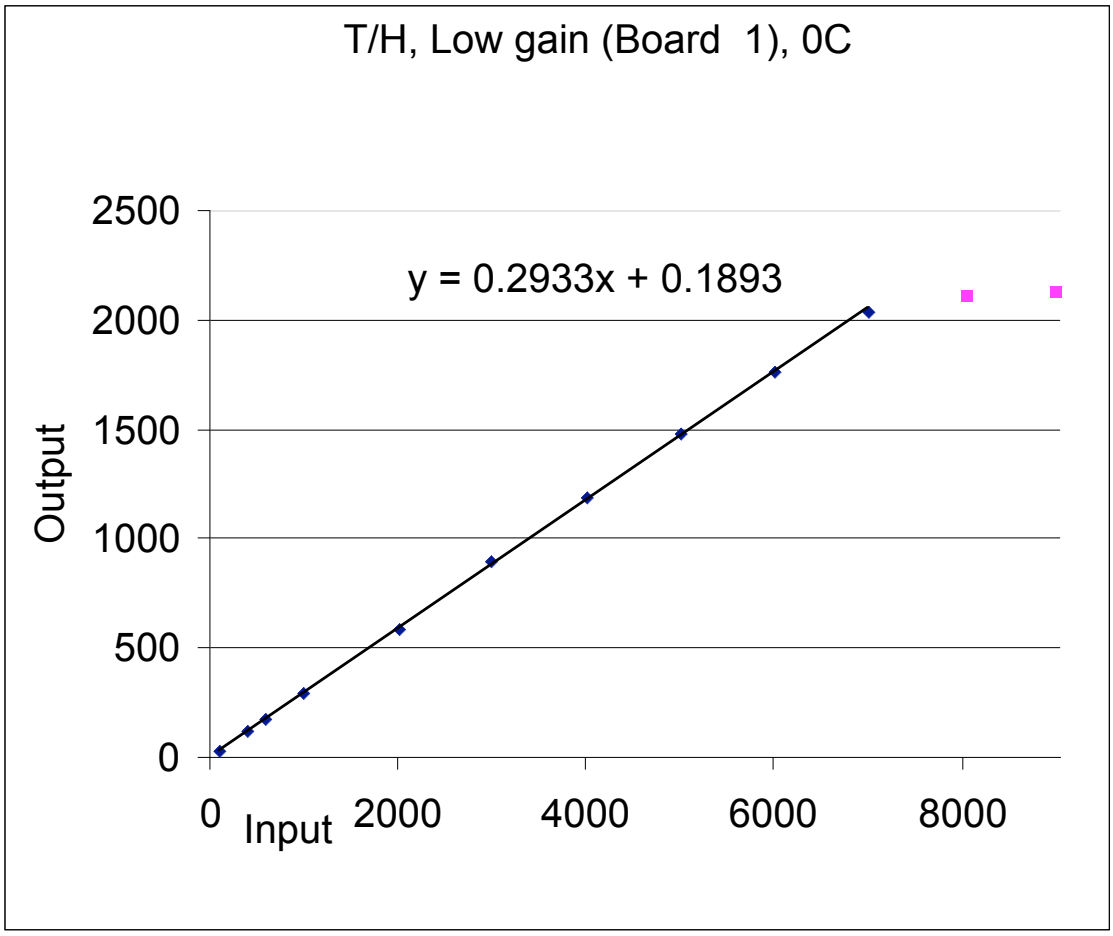
Track and Hold, High Gain Channel (Board 1):
Temp: - 20 C

MIP	Input Charge, PC	Input (mv)	T/H High Gain, mv
0.1015781	0.06501	1.97	20.5
0.5006719	0.32043	9.71	111.3
1.0260938	0.6567	19.9	230.8
2.0057813	1.2837	38.9	447
2.990625	1.914	58	670
4.00125	2.5608	77.6	897
5.0170313	3.2109	97.3	1116
6.0121875	3.8478	116.6	1332
6.9815625	4.4682	135.4	1538
8.0282813	5.1381	155.7	1755
9.0440625	5.7882	175.4	1976
10.039219	6.4251	194.7	2079



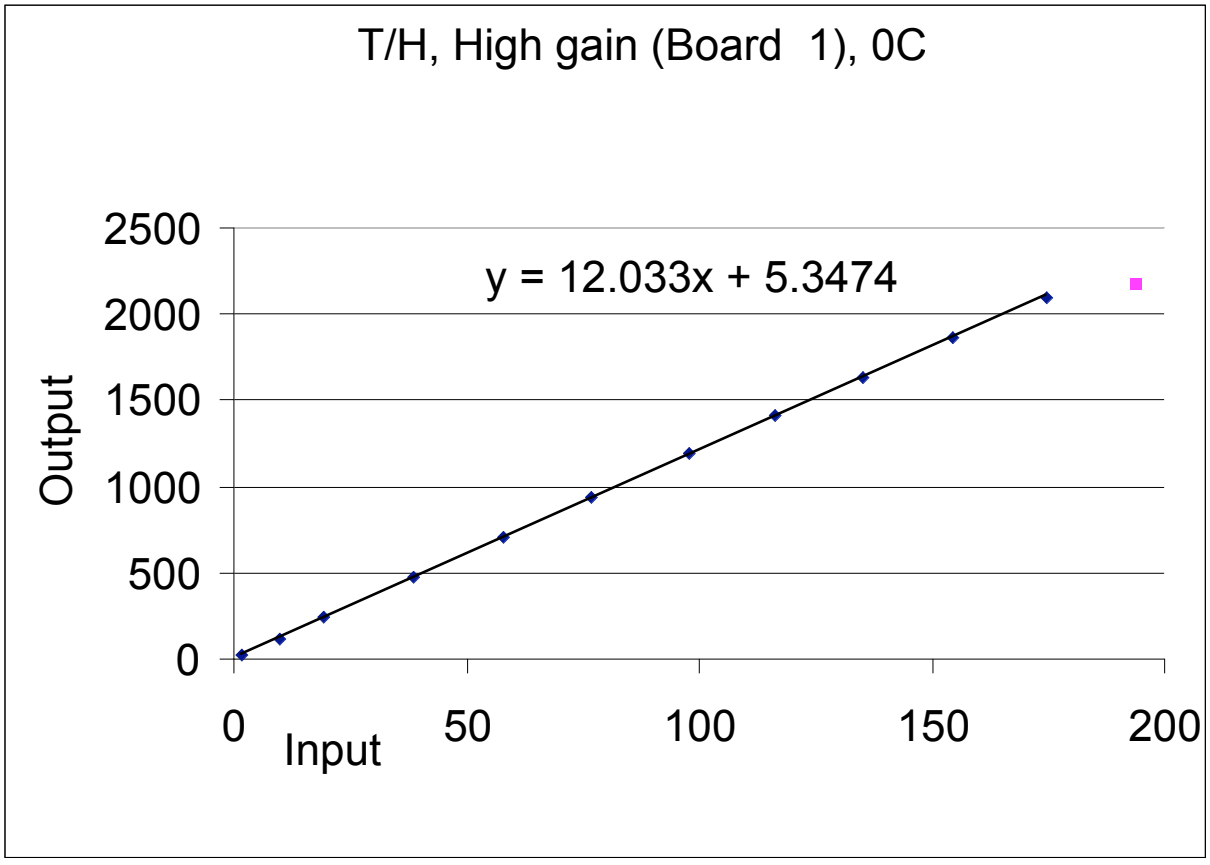
Track and Hold, Low Gain Channel (Board 1):
Temp: 0 C

MIP	Input Charge, PC	Input (mv)	T/H, Low gain, mv
5.1820313	3.3165	100.5	28.26
20.619844	13.1967	399.9	115.4
31.035469	19.8627	601.9	174.5
51.717188	33.099	1003	289.9
103.84688	66.462	2014	585.8
154.73906	99.033	3001	893.9
207.38438	132.726	4022	1186
258.32813	165.33	5010	1477
309.68438	198.198	6006	1764
360.9375	231	7000	2039
414.66563	265.386	8042	2111
464.68125	297.396	9012	2123

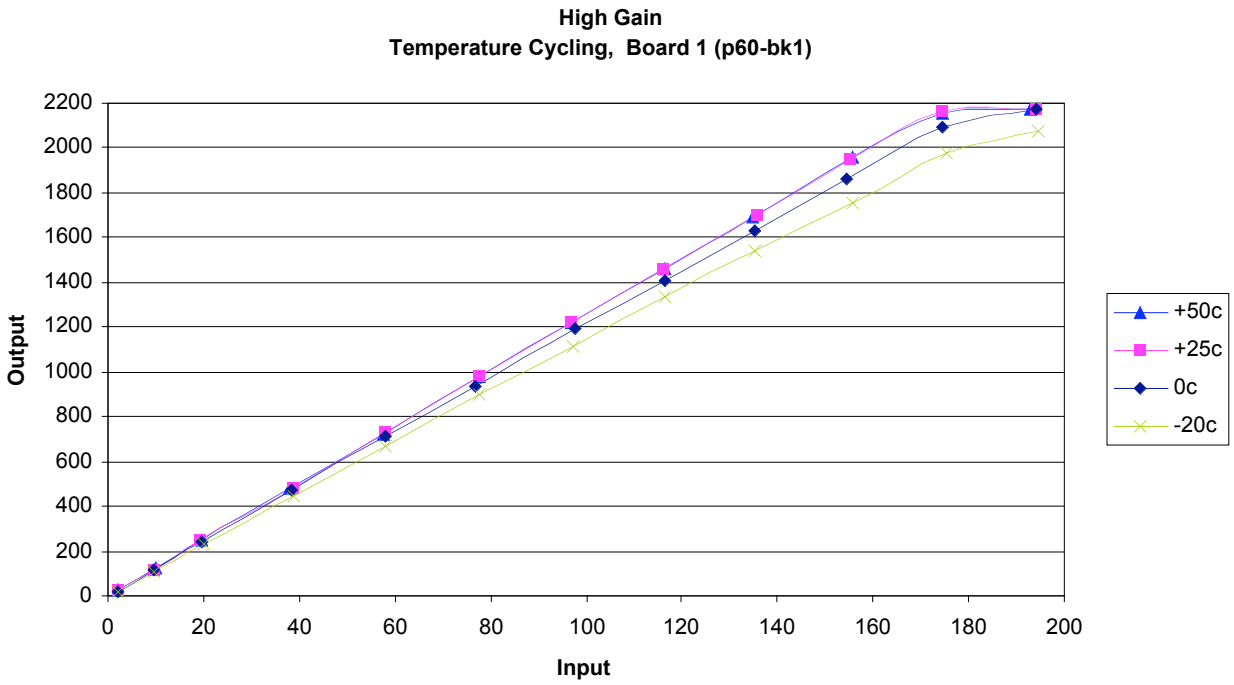


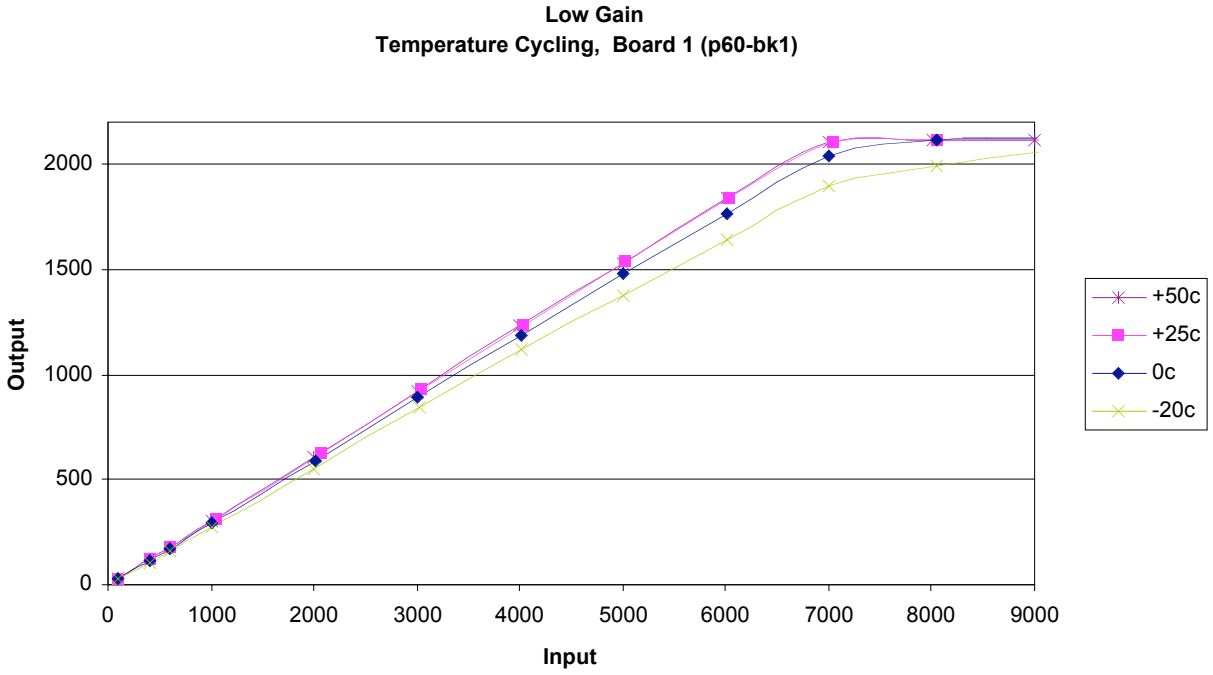
Track and Hold, High Gain Channel (Board 1):
Temp: 0 C

MIP	Input Charge, PC	Input (mv)	T/H, High Gain, mv
0.0969375	0.06204	1.88	20.44
0.4986094	0.31911	9.67	117.66
1.0054688	0.6435	19.5	238.7
1.9903125	1.2738	38.6	471
2.9957813	1.9173	58.1	710
3.9703125	2.541	77	938
5.0479688	3.2307	97.9	1193
5.9967188	3.8379	116.3	1408
6.9815625	4.4682	135.4	1632
7.9715625	5.1018	154.6	1864
8.9976563	5.7585	174.5	2097
10.013438	6.4086	194.2	2173



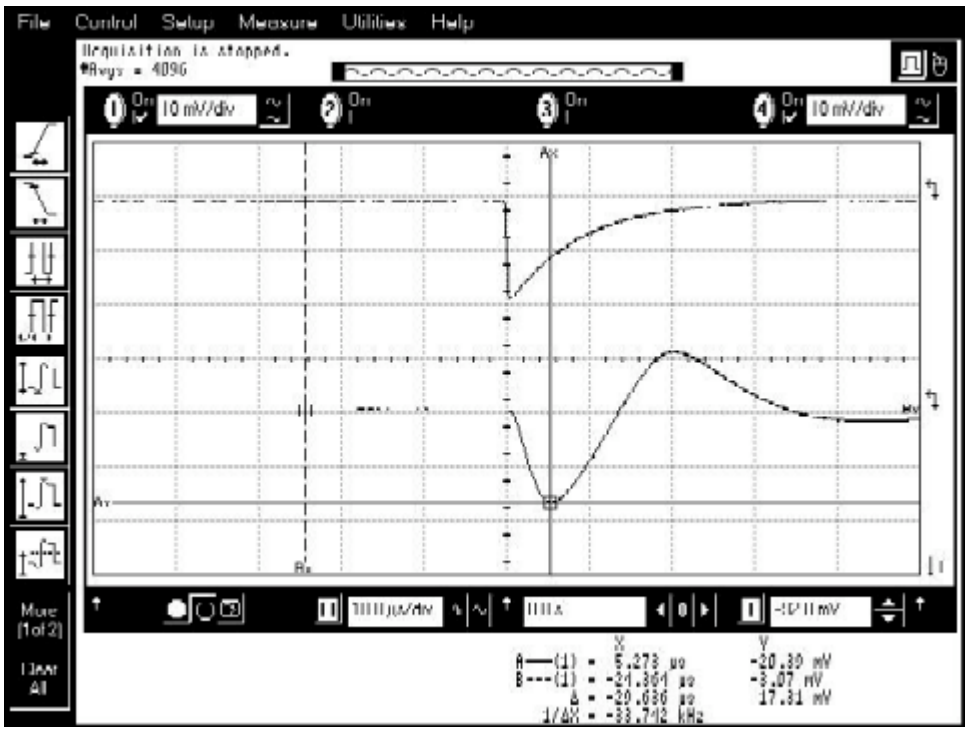
The Track and Hold output for all the temperatures is summarized below in the plots for low and high gain channels.





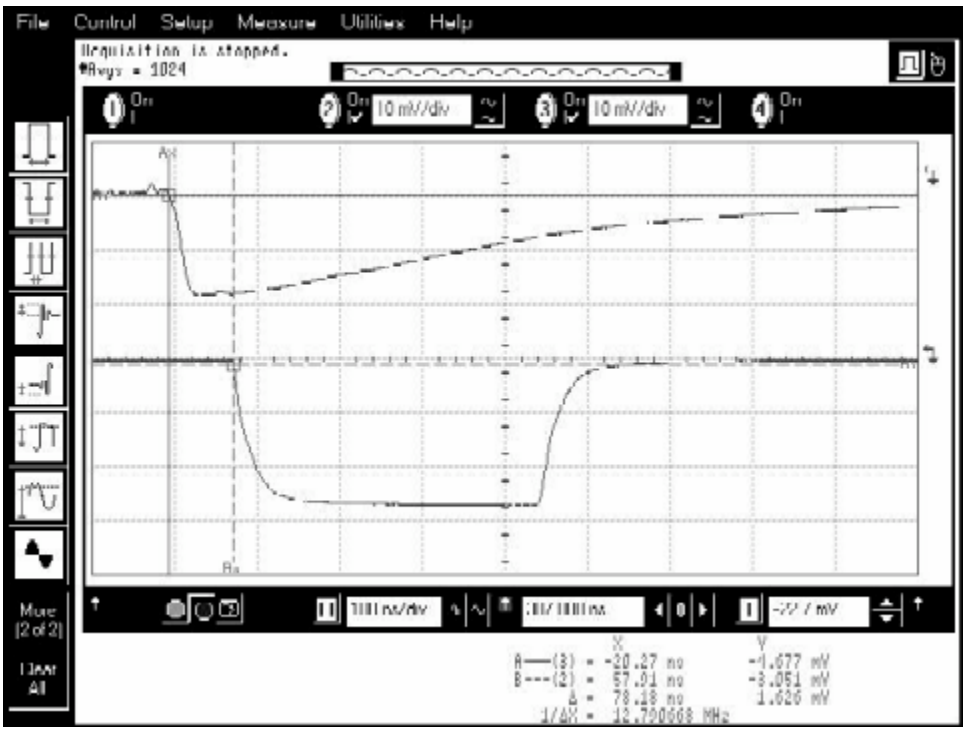
4.5 Test with PMT:

The ASIC was connected to the PMT and the shaping Amp output observed. The Shaping amp output was found to be clean and stable even for 1 MIP signal. The noise floor was found to be very much less than the 1 Mip signal, a picture of the scope with PMT hooked up is shown.

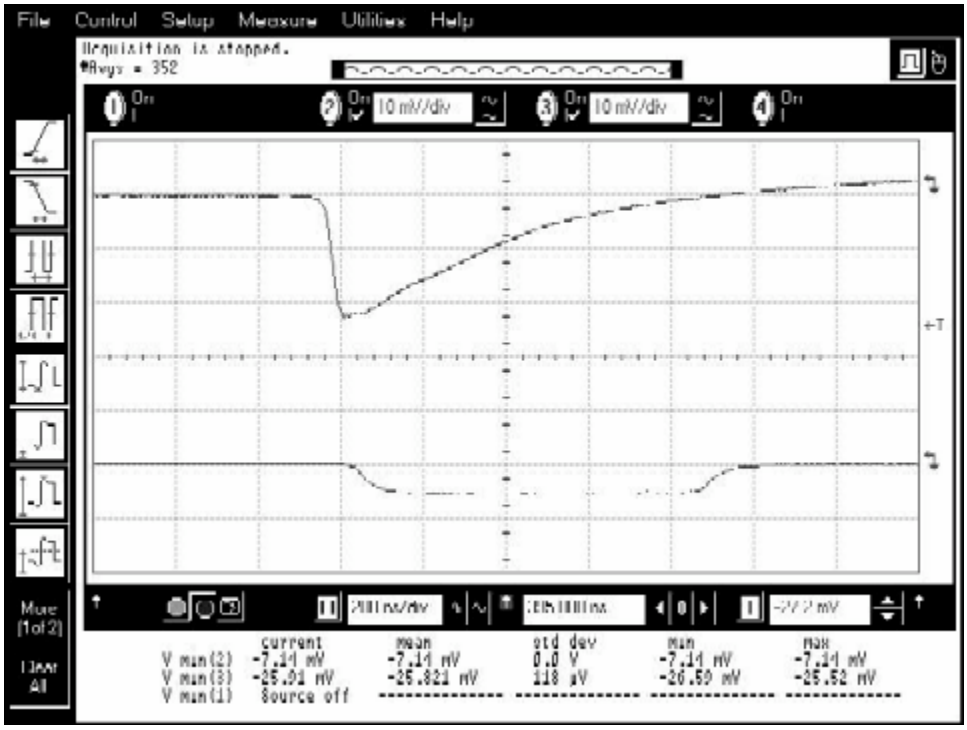


4.6 VETO Generation:

The VETO output for 1 MIP is shown in the scope pictures. It is seen that the delay is less than 100 ns. However, this delay is expected to increase after going traversing over the PCB tracks to the GARC chip and after going through the differential receivers



4.7 VETO Generation (cont):



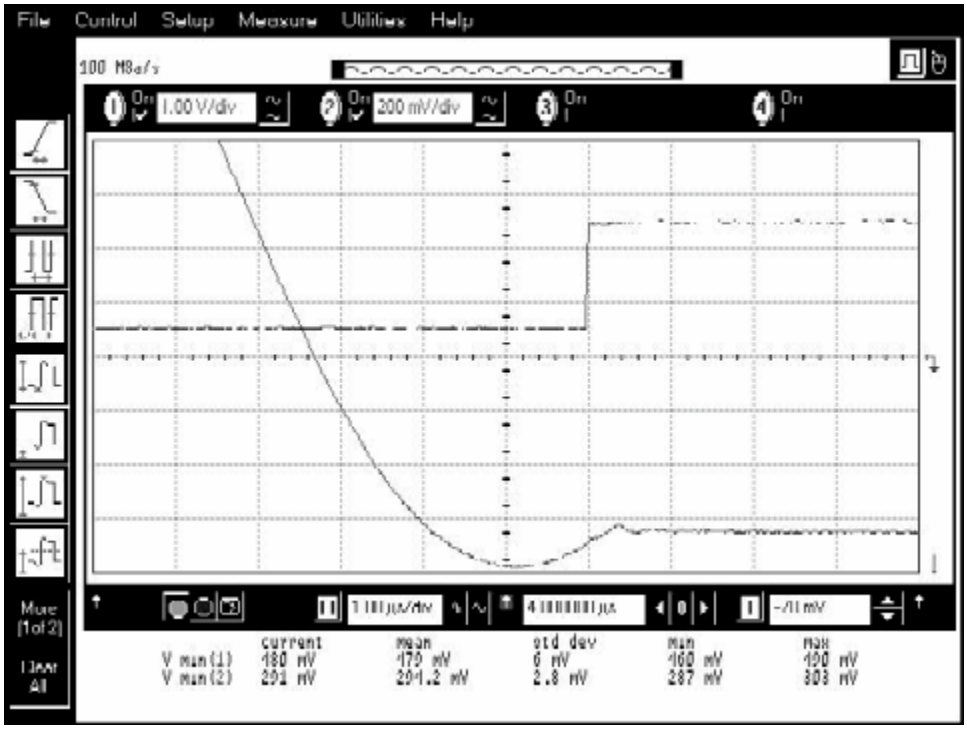
4.8 High Voltage Protection:

One end of a series cap of 1nv was charged to a high voltage and then shorted while the other end of it was connected to the ASIC input. It was found that even with a 3kv volt, the ASIC survived which is almost six times the requirement since the max PMT HV is 1500v and the cap is 340 pf.

The cap value was then increased to 5nf, and the chip was found to survive 2KV, at 3kv the chip was however damaged.

4.9 Sample Hold

The differential Hold input did not work as expected since the VDD supply is loaded by the digital control block. However, by increasing the differential input to around 1.5 v the, hold operation took effect and a sample and hold output was available at the ASIC output pin.



4.10 LLD and HLD Discriminators:

The LLD and HLD triggers were also tested and found to work with latencies of around 100 ns.

4.11 Mux and Channel Select

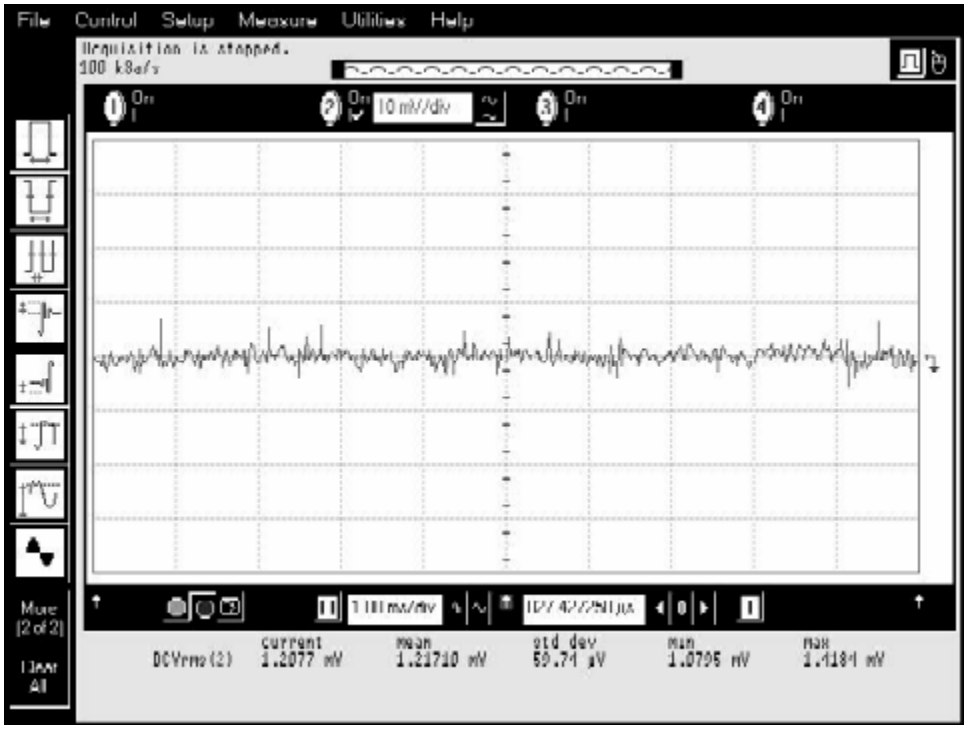
The multiplexers and channel select were found to be working as the low and high energy channels could be selected by applying the right digital level at the channel select pin.

4.12 Noise

The noise was measured on the SA output of board 1 while shielded in an aluminum box with the input open and the shaping amp mux switched to the high gain channel. The mean value of the DCVrms scope function was used. The noise voltage of 1.3mv rms was measured.

1 mip ⇔ 20mv at input
Therefore for a Shap Amp (SA) gain of 7,
1 mip ⇔ 140 mv at SA output
Therefore,
1.3mv rms noise at SA out ⇔ 1.3 / 140 = 0.009 mips

The requirement on the ASIC is that noise be less than 0.1 mip.



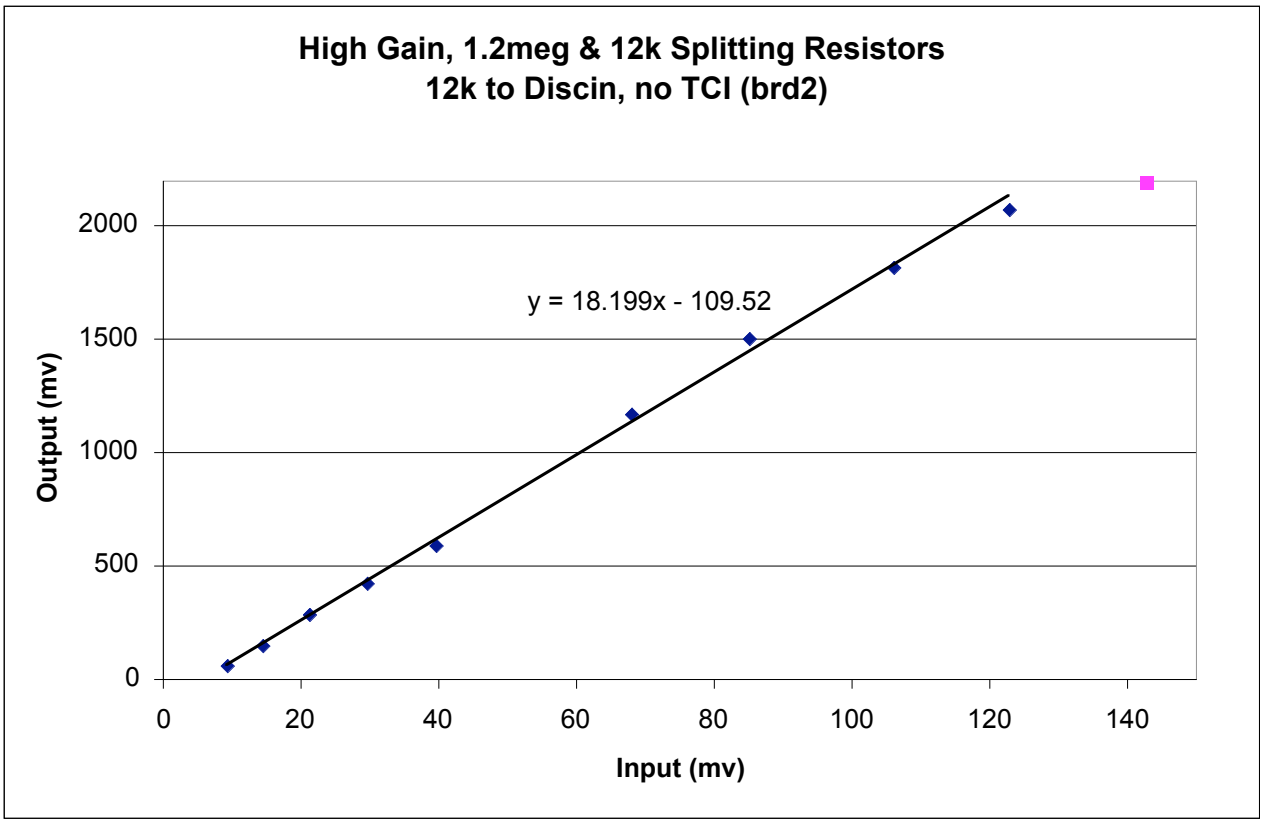
4.13 Linearity Tests with PMT

To further check the basic circuit design concepts, the GAFE1 ASIC was tested with PMT. The PMT used was, part # ZL0609, R4443 Q-2, with a gain of 6.2 as measured by Alex Moiseev. The PMT was stimulated with a red LED with a pulse of 170 ns width, and the amplitude of the pulse to the led was varied to stimulate the PMT up to 1000 MIPs approximately. For the tests reported below, the output of the PMT was connected through approximately 10 inch cable length to the node common to the two charge splitting resistors. The charge splitting resistors that were used were 12 to the "salo" input

and 1.2 Meg to the "sahi" input. The input capacitance of 33pf was not used as the cable capacitance was estimated to be even a little more than that. In addition a 10x scope probe with a capacitance of 10.8Pf was connected to the input to measure the PMT output. Since the PMT output has statistical fluctuations, averaging of the waveforms was used on the scope.

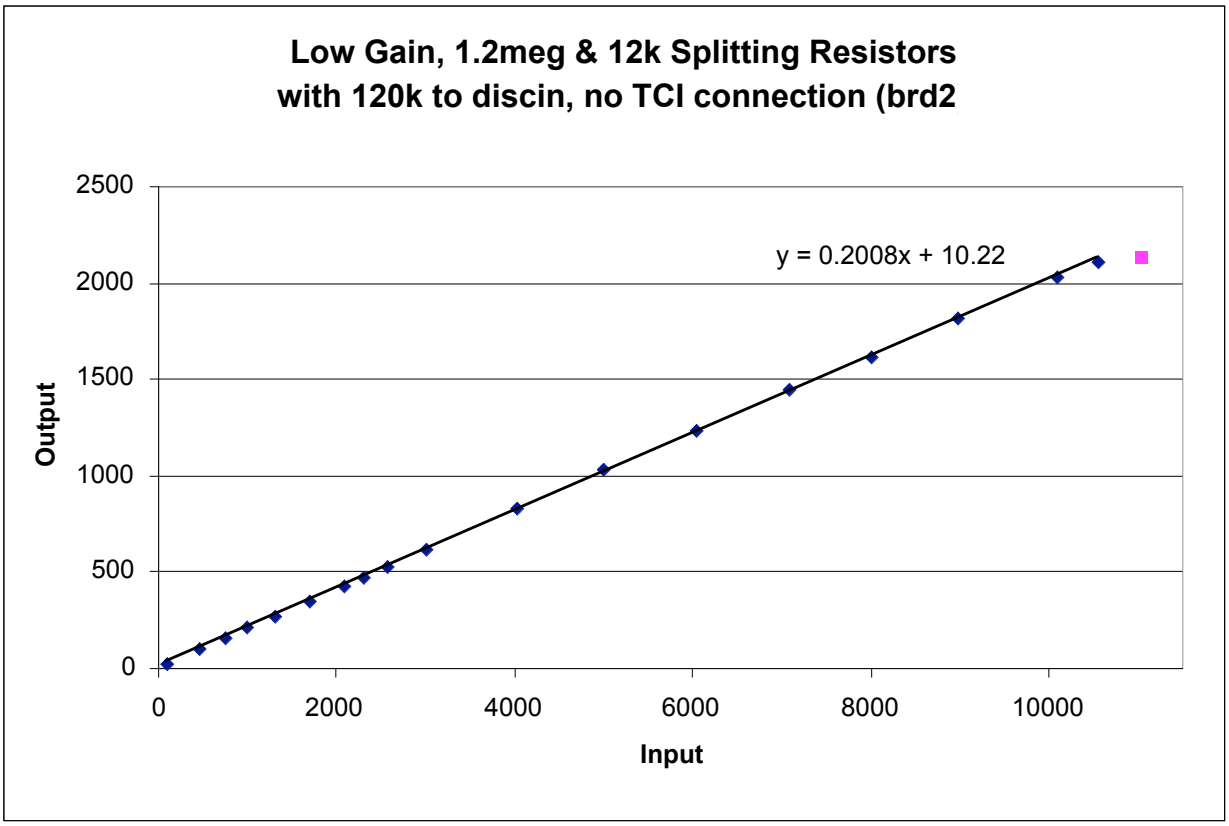
The measurements for the high gain channel are shown below. The resistances used were 12 to the salo input, 1.2Meg to the sahi input, 12k to the discin input, and the test charge injection pad, tci, was left unconnected.

PMT Out (mv)	High Gain (mv)
143	2193
123	2070
106	1820
85	1507
68	1166
39.57	591
29.76	422
21.4	282
14.6	143
9.5	55



The measurements for the Low gain channel are shown below. The resistances used were 12 to the salo input, 1.2Meg to the sahi input, 120k to the discin input, and the test charge injection pad, tci, was left unconnected.

PMT Out (mv)	SA low gain (mv)
11033	2127
10565	2112
10093	2032
8988	1817
7995	1615
7085	1445
6050	1237
5008	1027
4032	830
3005	619
2560	529
2309	475
2085	429
1700	347
1320	273
1002	208
762	158
470	98.9
99.3	20.72



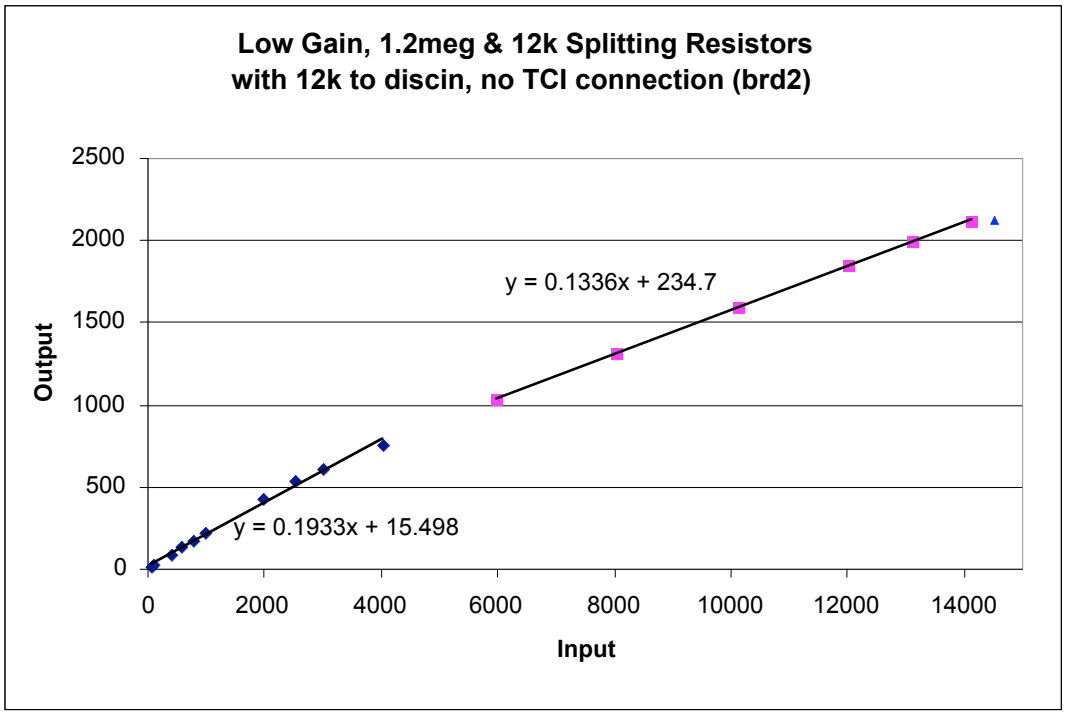
The above two graphs show that the charge splitting is linear all the way upto the full scale in each of the low and high energy channels. The ratio of the gain in the two channels is, 18.199 / 0.2008 = 90.6, which is close to that predicted by simulations when using charge splitting resistors of 12k and 1.2Meg.

Effect of Protection Pads on the linearity:

The pads on the ASICs have protection diodes which clamp the signal to the ground and supply if the input signal were to exceed these voltage limits. For large signals, these diodes kick in and affect the linearity. For the pad to which the "salo", the low energy channel input, this is not a problem as the protection diodes provided added path to AC ground. However, the pad for the discin, does have an effect on the linearity as that is not a charge input, but a high impedance input to the comparator and voltage amplifier.

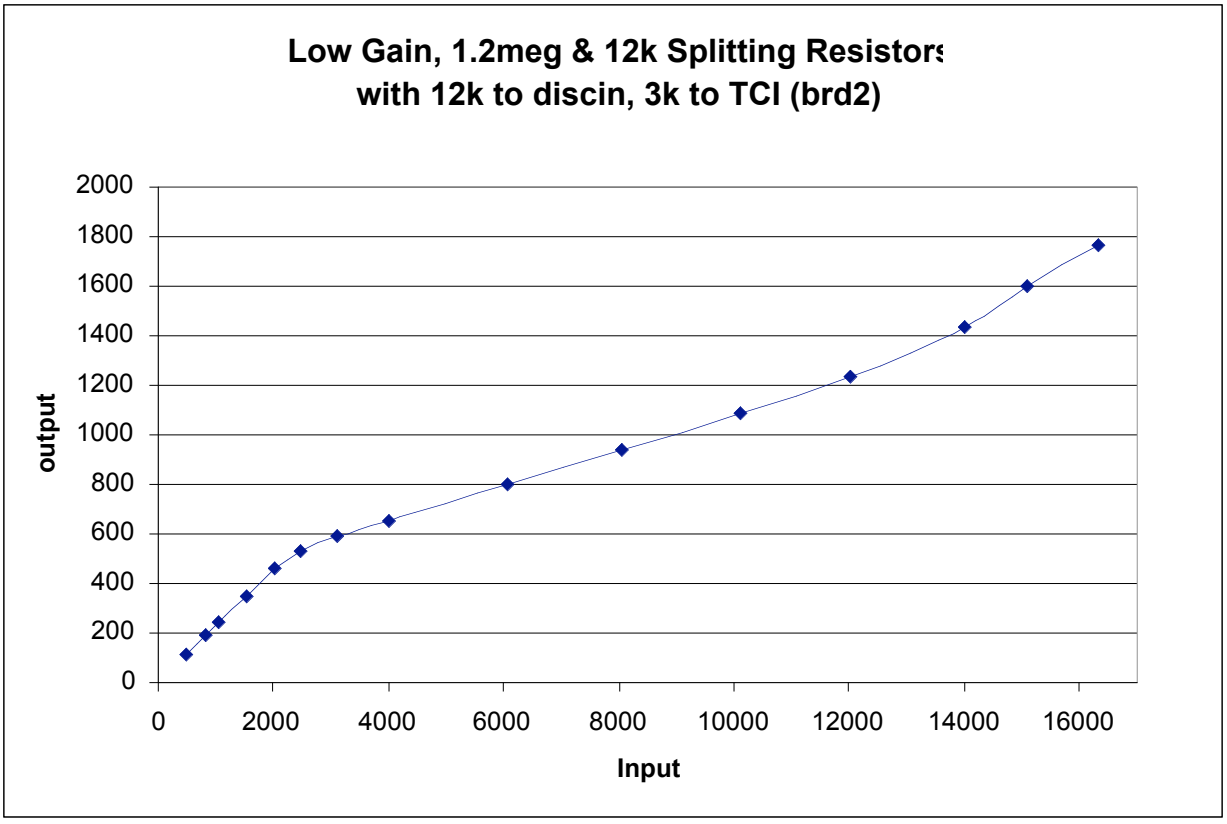
The readings shown in the table on the left were taken with similar settings as for the preceding graph, but with 12 k to discin, instead of 120K used earlier. The charge splitting resistances of 12k and 1.2Meg were used as before.

PMT Out (mv)	SA low gain (mv)
14519	2126
14145	2117
13106	1994
12032	1845
10131	1588
8051	1310
5987	1034
4026	757
3020	609
2520	530
1980	422
1000	216
797	170
595	128.5
400	88
111	25.25
62	14.18



Below are shown the readings for the test charge injection also connected by a 3.3k to the input in addition to the 12k to discin. The charge splitting resistances of 12k and 1.2 Meg were used.

PMT Out (mv)	SA low gain (mv)
16342	1767
15096	1596
14016	1433
12031	1237
10095	1084
8060	940
6050	801
4022	655
3106	588.5
2470	533
2035	464
1518	349
1062	244
813	187
492.6	114



From the above graphs we see that the 3k connection to the "tci" input seems to have the greatest effect on linearity, this is because of the protection diodes kicking in and providing a low impedance current return path to the input charge.

5. Test Summary

The GAFE1 version has the basic analog modules and also the first attempt to fabricate the digital core. The initial aim of this chip was to only test the analog modules, but since there was a lot of empty space on the die, the digital core was thrown in the last minute. As such the digital section was not verified after extraction and as discovered later was found to have errors. As a result of these errors, the digital supply was heavily loaded. Down to around 2 volts. However, the analog section could still be tested, and the digital logic outside the core digital block was found to be operational.

The analog section was tested for dynamic range, linearity, noise, veto discriminator delay, temperature variations, etc. The peaking time of the shaped pulses was found to be approximately double. This was attributed to the Nwell resistances being twice the designed value, the actual value being higher due to the shrinkage associated with the process of masking and fabrication. These resistances are being replaced with Poly resistances in the future version.

. The linearity, noise, Track and hold, discriminators and all other analog functions were found to be functioning as per design. The tests with PMT also showed performance as expected.

In conclusion, the testing of the GAFE1 ASIC demonstrates the suitability of the basic design utilizing charge splitting for PHA channels upto 1000 MIPs, and generation of VETO pulse within acceptable delay limits.